FPGA BASED CHIRP GENERATOR USING MEMORY BASED TECHNIQUE

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Abstract— The following content describe the generation of chirp signal using Memory Based Technology. The required parameters to generate chirp signal are received by the system through RS-232 serial communication protocol. Based on the input parameters FPGA generate the Chirp signal matches the input parameters.

Keywords— FPGA, Chirp Signal, Memory Based Technique.

I. INTRODUCTION

In RADAR radio signal are generally transmitted through the transmitter and echo pulses which are reflected from the objects are received by the receiver. By observing the distortion in echo pulses and time delay of the return echoes, the properties and dimensions of the object can be detected. The propagation of different frequencies varies in different materials. Some material may absorb maximum amount of energy and yield less echo distortion. Due to these reasons it is important to transmit a band of frequency over period of time, by doing so information which is not available for one frequency might get for another frequency.

A new RADAR technique called “Pulse Compression” which is “A Swept Wave” or “Chirp” signal consists time-varying frequency currently available for detecting objects. There are so many advantages by using this technique, especially the range and resolution of the target significantly improved when compare to conventional pulse method.

II. PROBLEM STATEMENT

There are different types of Chirp generator techniques explained in [1]-[2]. Memory Based Technique should aim for to generate chirp signal with any range of band of frequencies. The technique of generating chirp signal should be straightforward enough that implementation of this technique can be easily understood.

However, the generation chirp signal using Memory Based Technique explained in [1] is inefficient to generate any kind of chirp signal. Current memory based technique generate chirp signal with predefined range of frequencies i.e. the samples of chirp signal with predefined range frequencies will calculate initially and stores in the either Blocked RAM or Distributed RAM of FPGA.

To generate various range of frequency chirp signal by using current method need to store large amount of data samples and uses all the memory and resources of FPGA.

Modified Memory Based Technique can able to generate any sinusoidal frequency single by using less memory and resources of FPGA. The benefits of modified Memory Based Technique are it can generate any single tone frequency as well as chirp signal with various band of frequencies. The maximum frequency that can be generate is defined by the system clock.

III. MOTIVATION

Design chirp generator for “Synthetic Aperture Radar” as a key geometric data source for environmental monitoring. To synthesize high fidelity, long duration chirp waveforms, also known as Linear FM. They have an ideal rectangular spectrum to utilize the channel’s capacity and offer lowest power density. They are programmable at the same time suppress adaptively disturbances and noise.

All three main modulation modes can be applied at the same time.

1. Frequency Modulation.
2. Amplitude Modulation.
3. Phase Modulation.
The range of detection and the quality of resolution can be chosen accordingly by varying the pulse duration of chirp signal

IV. LITERATURE SURVEY

In present days commonly use radar are pulse type i.e. the system which transmit a large burst of radio frequency energy for a given interval and receives echo which are reflected from the target within range. From these reflected echoes, the position, size, type, and motion of the target may be determined. There are various applications in which pulse radar are used such as weather observation, airport flight control, travel assistance for the blind and collision detection devices. There are different techniques to synthesize chirp signals. Direct digital synthesizer is one of the technique through which waveforms can be synthesized form the phase of the signal [1]-[9]. In recent years parallel processing technique for high frequency conversion is the significant part of waveform synthesizing [3]. As memory is the one of the key factor in the system, Memory based Technique to Linear FM signal generator using with less memory utilization [1]. The Memory Based Technique explained in [1] can generate predefined linear chirp signal and cannot be programmable. This paper address the problems in Memory Based Technique and generalize the technique so that it can be programmable and can be synthesize any single tone frequency as well as linear FM signal with required band of frequencies.

V. IMPLEMENTATION

Radar systems frequently use pulse modulated signals which may also incorporate a linear frequency sweep (chirp) to enhance the performance of the system. A typical chirp radar pulse requires the generation of a pulsed RF signal where the carrier frequency is swept by several mega hertz over a typical time interval of 10 to 100 microseconds.

Implementation of a chirp signal generator on an FPGA based board is as follows:

1. Memory Based Technique is deployed as a core inside the FPGA.
2. Output frequency is controlled by the phase increment value (each value corresponds to particular frequency).
3. Depending on the chirp rate (rate of change of frequency w.r.t time) the phase increment value of the Memory Based Technique will be updated.
4. The required bandwidth will govern the DAC sampling rate to satisfy nyquist criterion.
5. This signal is passed through filter for conditioning and rejection of harmonics and other spurious signals before being produces at the output.

Memory Based Technique:

Memory Based technique is one of the method to generate Complex signals. Memory Based Technique employs look up table scheme

General Description:

In digital communication system Look Up Table (LUT) scheme plays an important role. The LUT schemes can be used for constructing digital down or up converters and implementing different kinds of modulation techniques such as PSK(phase shift Keying),FSK(Frequency Shift Keying) etc. Look up table stores samples of sinusoid signal. A digital integrator is employed to generate a equivalent phase parameter that is mapped by the look up table to generate required wave form

Theory of Operation:

From the Figure Input to the accumulator is Phase incremental value which decides the starting frequency. The output of the accumulator acts as a address to the look up table and extract the sinusoidal value stored in the table. The output of LUT is fed to the Digital to Analog Converter to generate Analog signal.

The phase incremental value is depends on the depth of LUT i.e. the number of sinusoidal samples stored in the Table. Output frequency depends on the phase incremental value, system clock and number of sample stored in the LUT.

\[ \text{fout} = \text{Fclk} \times \Delta \phi \]  \hspace{1cm} (1)

\[ \text{fout} = \left( \text{Fclk} \times \Delta \phi \right) / 2^n \]  \hspace{1cm} (2)

Where fout represent desired output frequency, Fclk represent System Clock and \( \Delta \phi \) represent phase incremental value

Phase incremental value is given by the following expression
\[ \Delta \phi = 2^n / \text{No. of Samples} \]  
Where \(2^n\) represents depth of look up table or total number of samples stored in the table.

**Calculations of LUT Values:**
Sinusoidal equation in analog domain is given by following equation:

\[ \sin(2\pi f_s \cdot t) \]  

From equation (2)

\[ \sin(2\pi f_s \cdot \text{Fclk} \cdot \Delta \phi / 2^n) \]  

The representation of equation (5) in discrete domain is given by

\[ \sin(2\pi f_s \cdot \Delta \phi \cdot n / 2^n) \]  

The range of \(\Delta \phi \cdot n\) term varies from 0 to depth of LUT.
The phase incremental value depends on the no. of sample values stored in the LUT. As depth of LUT increases the resolution of the frequency changes and the memory require to store the values will increase.
The change in the phase incremental value defines the output frequency. To generate monotonic sinusoidal signal the phase incremental value should be kept constant. Chirp signal can be generated by changing the phase incremental value at every instance of clock. In mathematical term the rate of change of phase will generate single frequency signal provided that rate of change of phase between two successive values constant. The rate of change of rate of change of phase will generate chirp signal.

**VI. RESULTS AND DISCUSSIONS**

**Single tone frequency:**

The Fig. 4 shows the 5 MHz signal with constant period by keeping the incremental value of phase constant.

**Chirp Signal:**

The Fig. 5 is a Linear FM signal (up conversion) swept from 0 MHz to 5 MHz. The duration of chirp signal is 10 usec. The repeating pulse is 2 msec.

**Frequency Vs Power:**

Frequency Vs power plot gives the power associated with each frequency present in the chirp signal. The plot as shown in the Fig. is pulse shape which represents the associate power of each frequency is same.

**DAC Output:**

The Fig. 8 shows the DAC output of chirp signal swept from 0 to 5 MHz. The duration of Chirp signal is 10 us.

**Specifications of Linear FM Chirp Signal:**
TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Frequency</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Sampling Interval</td>
<td>10 us</td>
</tr>
<tr>
<td>Chirp Bandwidth</td>
<td>5 MHz</td>
</tr>
<tr>
<td>Chirp Duration</td>
<td>10 us</td>
</tr>
<tr>
<td>Chirp Slope</td>
<td>5 MHz/us</td>
</tr>
<tr>
<td>Data Resolution</td>
<td>16 bit</td>
</tr>
<tr>
<td>Depth of LUT</td>
<td>36000</td>
</tr>
<tr>
<td>Accumulator Width</td>
<td>32 bit</td>
</tr>
</tbody>
</table>

CONCLUSION

In this paper FPGA based chirp signal is successfully implemented on both virtex 4 and Spartan 6. The memory based architecture has been synthesized and implemented on the FPGA platform. The digital data is converted into analog through 16 bit digital to analog converter. The output of DAC is passed through low pass filter for smoothening the signal.

Improvements can be done in generating Chirp signal such as increasing system clock frequency so that Chirp signal with higher band of frequencies can be generate, signal flattening technique can be employed before or after digital to analog converter.

REFERENCES