FPGA IMPLEMENTATION OF GENERALIZED HOUGH TRANSFORM

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Abstract - Hough transform is used for robust detection of line and circles in an Image. Hough Transform provides accurate results in case of noise and faulty input data of an image. This paper gives design of FPGA hardware implementation of Generalized Hough transform. Input image can be of maximum size of HD image. Xilinx 13.2 Design suite is used for simulation and XC6SLX45 FPGA device of SPARTAN-6 family is used as hardware.

Index Terms—Hough Transform and voting scheme, Xilinx simulation, FPGA Design

I. INTRODUCTION

In Hough transform input image which is represented using x-y plane is transformed into ρ-θ plane using following equation

$$\rho = X*\cos\theta + Y*\sin\theta \quad (1)$$

A perpendicular is drawn from origin to line present in an image. ρ is length of perpendicular and θ is angle made by perpendicular with x axis. By putting each (x, y) coordinate point in equation one, ρ-θ plane can be formed. Number of co-linear point of a line in X-Y plane are transformed to Sinusoidal curves that are intersects at common point (ρ', θ') in the parameter ρ-θ plane. ρ-θ plane is divided into accumulator cells representing one (ρ, θ) value of parameter space and it is considered as one vote. Accumulator cell getting maximum votes is nothing but parameters of line present in input image. Input color image is converted into gray binary feature image using MATLAB. Xilinx 13.2 design suite used for simulation and Programming language used is Verilog.

II. METHODOLOGY

FPGA register banks are used as Hough Transform matrix which stores all votes. Register bank memory is used to store Input image. After that Hough transform voting scheme is performed which gives local maxi-ma of Hough matrix this maxi-ma of Hough matrix is nothing but the parameters of the line in given input image if a line is present in an input image then all pixels representing line are having non zero intensity values are not considered for voting scheme of Hough transform. At first, initialize all Votes as zeros. Put value of very feature points (x, y) present in x-y plane in equation and find ρ value. Round that value to integer.

This ρ value is nothing but one vote of particular accumulator cell in Hough matrix. Whenever that ρ value is repeated increase its vote value by one using following equation

$$\text{Votes}(\rho', \theta') = \text{Votes}(\rho, \theta) + 1 \quad (2)$$

Here ρ', θ' getting max votes are nothing but required parameter of input image.

III. DESIGN STEPS

Synthesize complete code of system using Xilinx. Implement design by selecting proper hardware in Xilinx. Generate timing constraints of the project then assign appropriate I/o pin of hardware to project's I/P and O/P pins. Generate programming (.Bit) file. Now to download this programming (.Bit) file into Spartan device use Digilent Adept software, browse .bit file from project folder. After successful download of programming file reset device and run code. On led of port observe final rho value.

IV. RESULTS

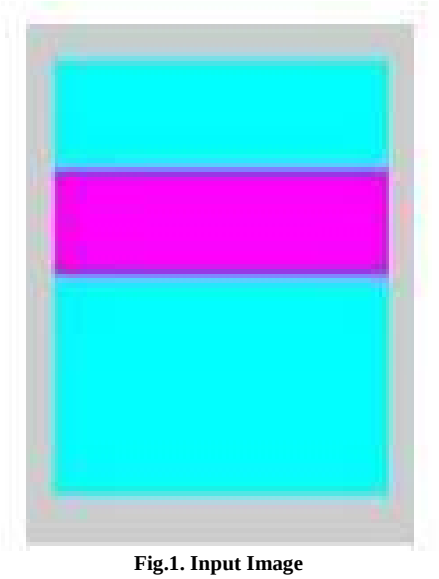

Fig.1. Input Image

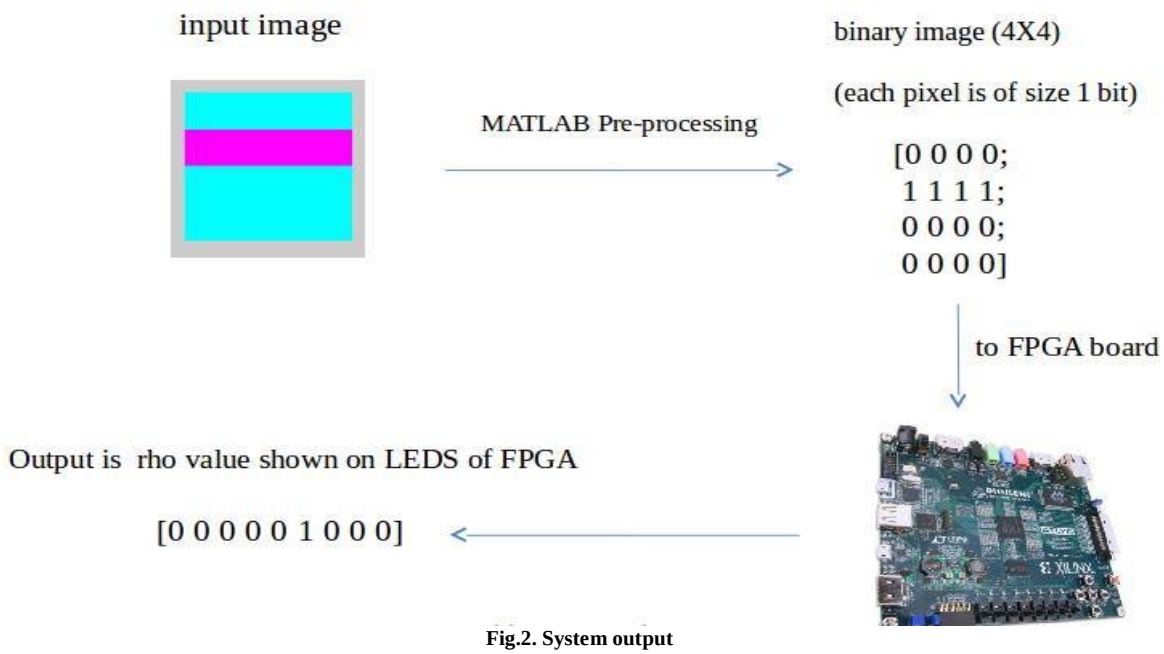

Fig.2. System output

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	516	184304	0%
Number of Slice LUTs	601	92152	0%
Number of fully used LUT-FF pairs	468	649	72%
Number of bonded IOBs	13	498	2%
Number of BUFG/BUFGCTRLs	1	16	6%

Fig.3. Device Utilization

Image shown in figure one given as input to the MATLAB for processing, Image specification required for Xilinx simulation are observed form MATLAB result. Output of the system is explained in fig. 2. Device utilization details are given in fig. 3.

V. ALGORITHM

- Define I/O ports of the system
- Define port's signal flow direction and their respective data-types
- Define various wires, registers and constants required in code Using Cardiac core find sine and cosine values of input angles
- Define always block and rotate is at rising edge of clock
- Initialize all the counters used in loops
- Perform voting procedure and store votes in Registers

CONCLUSION

Hough transform is important technique used to detect lines in an image. FPGA can be used as hardware accelerator and it provide real time implementation of Hough transform. Xilinx simulation result is verified on hardware using Spartan-6 XC6SLX45 FPGA board. Images with different sizes are tested on hardware. Images with complex image sizes require more Computations and processing time so this system is useful for images with small sizes.

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