**VLSI DESIGN OF BARREL SHIFTER USING COMPLEMENTARY AND PSEUDO NMOS LOGIC**

1,2,3 Dhananjay Jadhav, 2Mithilesh Muley, 3Mangesh Ashtankar

1,2,3 Dept. of Electronics Engg. Nagpur, India.

**Abstract**—The purpose of the paper is to design the barrel shifter using complementary logic and pseudo dynamic logic. The barrel shifter is essential element in ALU. It is used for the shifting operation in left direction or in right direction. The design of barrel shifter and simulations are done on TANNER EDA 13.2 tool. The methodology in this work are (1) CMOS static logic (2) Pseudo NMOS logic. This work evaluates on 250nm and 180nm technology. It is design to reduce area and power of barrel shifter in ALU. At the end, both the logic structures are analyzed and optimize area logic is purposed.

**Index Terms**—Barrel shifter, Tanner EDA tool, Static CMOS logic, Pseudo NMOS logic, 250nm, 180nm

I. **INTRODUCTION**

Barrel shifter is essential components in ALU. Barrel shifter is often used for shifting operation like shift right logical, shift left logical, shift left arithmetic, shift right arithmetic, right rotate, left rotate. The architecture of barrel shifter can be designed by using 2:1, 4:1, 8:1, 16:1 Mux trees[8]. Barrel shifter is most essential element in DSP applications[3]. Barrel shifter is designed using Mux trees to use it in repetitive form so that power consumed by the barrel shifter should minimum. Our work is divided into two sections. At first, the multiplexer is designed with complex logic structure on 250nm and 180nm technology. And secondly, by using Mux block barrel shifter is designed on 250nm and 180nm technology. Complex logic structure involves following techniques (1) Static CMOS logic (2) Pseudo NMOS. Result comprises of comparison of both technology techniques and simulation of above all logics which shows the optimized area which is helpful in low power ALU design.

II. **MULTIPLEXER**

Multiplexer is one of the basic components in digital circuits. It consists of 'n' number of input and single output. It has wide range of applications. In this project mux is designed and implemented on TANNER EDA 13.2 tool. This Multiplexer is later used to design barrel shifter using static CMOS logic and Pseudo dynamic logic on 250nm and 180nm technology file. The working truth table of multiplexer is as shown in below table.

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>A</th>
<th>B</th>
<th>output</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>A</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>X</td>
<td>A</td>
</tr>
<tr>
<td>3</td>
<td>X</td>
<td>1</td>
<td>B</td>
</tr>
</tbody>
</table>

Table 1 Truth table of Multiplexer

Barrel shifter is combinational logic circuit with ‘n’ number of data inputs and data outputs and set of control inputs which are used to perform shifting operation. Barrel shifter is designed using Multiplexers. Barrel shifter design is for natural size like (2,4,16).This project is done on 8 bit barrel shifter which can Shift input by 0,1,2,3,4,5,6,7, bit. Four select lines are used as it is 8 bit barrel shifter i.e. S0, S1, S3. Basically barrel shifter is used with logical left shift operation which is controlled by select inputs. Select lines are used to specify the amount of shift only, For example, consider a 4 bit barrel shifter, with input A, B, C, D. The shifter can cycle through the order of bit ABCD i.e. It can shift all output through three positions[1]. It is designed using three types of complex logic structures which are efficient in reducing the power consumption of the barrel shifter. These logic styles are as given below.
The number of Multiplexer is calculated by following formula \([n \log_2 (n)]\), for \(n\) bit word.

- 16-bit — \(16 \log_2 (16) = 16 \times 4 = 64\)
- 8-bit — \(8 \log_2 (8) = 8 \times 3 = 24\)

A. Static CMOS Logic
A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN). The below figure 2 shows a generic ‘N’ input logic gate where all inputs are distributed to both the pull up and pull down networks. The function of pull up network is drive the Vdd towards output and function of the pull down network is to supply Vss to output. The noise margin of the static CMOS logic is high. The schematic diagram of 2:1 Mux is as shown in fig.2

B. Pseudo NMOS Logic
In pseudo NMOS logic all the pull up network is replaced by single PMOS. Here the load device is single P transistor with gate connected to ground. So the area required is less than that of the static complementary network. The gain of the pull up has to decrease to provide the adequate noise margin. The construction diagram 2:1 Mux using the pseudo NMOS logic is shown below in fig.3

IV. PROPOSED BARREL SHIFTER
After analyzing all two technologies, it shows that complementary logic uses both pull up network as well as pull down network so that number of CMOS required is more. In pseudo NMOS logic all the PMOS are replaced by the single PMOS, hence the no. of MOS required is reduced. As the numbers of Transistors are reduced the power consumed by the CMOS is also reduced.

V. SIMULATION AND PERFORMANCE ANALYSIS OF BARREL SHIFTER
Barrel Shifter is designed and simulated using the TANNER EDA 13.2 tool at 250nm and 180nm at Vdd level 5V, 3.3V. At first, 2:1 Mux is designed on both technologies i.e. 250nm, 180nm, using both complementary logic and Pseudo NMOS logic. The Simulated waveforms of the 2:1 Multiplexers are shown below in fig. 4 and 5, Secondly by using this MUX block barrel shifter is designed on both technologies as well as logic structures.

A. Area And Power Analysis
Area plays a vital role in digital circuit applications. In complementary logic number of NMOS is equal to
Number of PMOS which requires large area on chip of ALU. As the numbers of MOS are reduced in Pseudo NMOS logic, ultimately Area is also optimized. Therefore the area of barrel shifter is also reduced which helps to reduced the area of chip of ALU. As the area is optimized the speed of the operation is increased. Number of MOS required to each circuit design is as shown in table 2.

<table>
<thead>
<tr>
<th>Design</th>
<th>Number of MOS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Static CMOS Logic</td>
</tr>
<tr>
<td>2:1 MUX</td>
<td>8</td>
</tr>
<tr>
<td>4:1 MUX</td>
<td>16</td>
</tr>
<tr>
<td>8-Bit Barrel Shifter</td>
<td>192</td>
</tr>
</tbody>
</table>

Table 2 MOS Requirement for logic design

The power analysis is carried on 8 bit barrel shifter which is designed using complementary logic and Pseudo NMOS logic structures on TSPC 250nm & 180nm file over the transient time period of 1000 nanoseconds with respect to VDD = 5V and VDD = 3.3V respectively. The Average power dissipated by the barrel shifter is shown in Graph 1.

CONCLUSION

In this Paper, the barrel shifter is designed using complex logic structures and area of barrel shifter is reduced. By using Tanner EDA 13.2 tool power consumed by each logic on 250nm and 180nm is calculated and the reduced area and power barrel shifter is proposed.

RESULT

In VLSI, the major aspects of designing are Power, Speed and Area of the circuit. According to the design and simulation it is found that the area required for designing 8 bit barrel shifter using Pseudo NMOS logic reduces up to 62.5% than static CMOS Logic. In Power analysis, the average power dissipated in Static CMOS logic is less than Complementary logic by 1.45% on 250nm, while 1.31% on 180nm technology.

REFERENCES


★★★