A REVIEW PAPER ON IMPLEMENTATION OF FULL WAVE RECTIFIER WITHOUT DIODE USING OPERATIONAL TRANSconductance AMPLIFIER IN CMOS TECHNOLOGY

P.V.UPADHYE, G.M.ASUTKAR, A.C.KAILUKE

M.Tech PIET Nagpur, Professor; PIET Nagpur, Assistant Professor, PIET Nagpur

Abstract- This paper presents comparative study of Various design concepts of Operational Transconductance Amplifier (OTA). A comparison of various OTA design technologies used for the design is carried out in the paper. It also compare OTA parameters such as power supply, Gain, Gain Margin, Phase margin, Slew rate for various designs. Various applications of OTA such as full wave rectifier, OTA-based Non-Inverting and Inverting Precision Full-Wave Rectifier, High Performance Precision Rectifier for Analog Signal Processing, Current controlled precision rectifier circuits are also compared in this paper.

Index Terms- CMOS, full-wave precision rectifiers, Operational Transconductance Amplifier (OTA)

I. INTRODUCTION

Due to recent development in VLSI technology the size of transistors decreases and power supply also decreases. The OTA is a basic building block in most of analogue circuit with linear input-output characteristics. The OTA is widely used in analogue circuit such as neural networks, Instrumentation amplifier, ADC and Filter circuit. The operational Transconductance Amplifier (OTA) is basically similar to conventional Operational Amplifiers in which both having Differential inputs. The basic difference between OTA and conventional operational Amplifier is that in OTA the output is in form of current but in conventional Op-Amp output is in form of Voltage.

II. CIRCUIT DESCRIPTION

The proposed non-inverting precision full-wave rectifier circuit is shown in Fig. 1. It consists of a single OTA with three outputs (two positive outputs and one negative output) as an active element, two complementary MOS transistors and a resistor. The OTA is used as a voltage to current converter (to change the input voltage, Vin, into output currents Io1, Io2, Io3.)

Complementary MOS transistors work as a voltage controlled switch. The resistor RL is used as a current to voltage converter, which converts the rectified currents into output dc voltage, Vout. The relations of the positive and negative polarity input voltage and output currents of the OTA can be expressed as:

\[ \text{If } V_{in} > 0 : \]
\[ I_{o1} = +g_{m} V_{in} \]  
\[ \text{If } V_{in} < 0 : \]
\[ I_{o3} = -g_{m} V_{in} \]

For switching the two CMOS transistors (Mn and Mp), voltages ±Vsat are provided at their gates by connecting them to a positive output terminal of the OTA. Vsat corresponds to saturated voltage. Here, +Vsat equals to VDD and −Vsat to Vss i.e., biasing voltage of the OTA. The voltage ±Vsat produced at the gate of two MOS transistors will be (+g_{m} R_{p})V_{in}. Here R_{p} = R_{o} || R_{GP} || R_{GN}; R_{o} is the output terminal resistance of the OTA, and RGP and RGN are the gate resistances of the Mn and Mp transistors respectively. All these three resistances are quite high, resulting in saturation at this output terminal of the OTA.

Fig. 1. Proposed OTA-based non-inverting full-wave precision rectifier.

Depending upon the signal polarity (positive or negative) the voltage at the gates is +Vsat or −Vsat, respectively. The operation of the proposed circuit is as follows: In case of positive half cycle input voltage, Vin > 0 and +Vsat = VDD. Mn is ON (Mp is OFF). The output current Io1 (= g_{m} V_{in}) will flow through the load, RL, resulting in positive polarity voltage at Vout. In case of negative half cycle input voltage, Vin < 0 and −Vsat = Vss, Mp is ON (Mn is OFF). The output current (Io3 = −g_{m} V_{in}) will flow through the load, thus inverting the negative cycle of input.
Unidirectional current flows through the load in either case, resulting in a full-wave rectified output. Using (1) and (2), the relation between the input and the output voltage of the proposed rectifier can be obtained as:

\[ \text{Vin} > 0 : \text{Vo} = + gmRL\text{Vin} \quad (3a) \]
\[ \text{Vin} < 0 : \text{Vo} = - gm RL\text{Vin} \quad (3b) \]

Equation (3) shows that the transconductance gain of the OTA can control the rectified output voltage. Thus, the circuit can provide a control over the average (dc) output. Using eqn. 3 and \( gm = RL \), the relation between input and output voltages of the proposed non-inverting rectifier can be obtained as:

\[ \text{Vin} > 0 : \text{Vout} = + \text{Vin} \quad (4a) \]
\[ \text{Vin} < 0 : \text{Vout} = - \text{Vin} \quad (4b) \]

The inverting full-wave rectifier circuit can be realized from Fig. 1 by simply reversing the connection of positive and negative output terminals of the OTA, which are connected to the complementary MOS transistors (i.e. \( M_n \) and \( M_p \)) as shown in Fig. 2. The relation between input and output voltages would become:

\[ \text{Vin} > 0 , \text{Vout} = -\text{Vin} \quad (5a) \]
\[ \text{Vin} < 0 , \text{Vout} = \text{Vin} \quad (5b) \]

The design of this Operational Transconductance Amplifier (OTA) is done using Cadence Tool. The simulation results are done using Cadence Spectre environment using UMC 0.18 \( \mu \)m CMOS technology. The simulation result of the OTA shows that the open loop gain of approximately 71 dB. The OTA has GBW of about 37 KHz. The Table II shows that the simulated results of the OTA. The AC response which shows gain and phase change with frequency is shown in figure 2. Figure 3 shows the DC sweep response of This OTA. The simulated results of this OTA shows that PSRR of 85 dB and CMRR of 90 dB.

[2] In this paper two stage OTA is optimized and simulated in 0.18\( \mu \)m and 0.35\( \mu \)m technology. Power supply of the architecture is 1.8V. Gain is 47.86 dB, gain margin is 15.40 dB and phase margin is 217.530. Slew rate is 37.58 V/\( \mu \)s and power dissipation is 1.3 mW and Power supply of the architecture is 3.3V. Gain is 46.75 dB, gain margin is 16.94 dB and phase margin is 2250. Slew rate is 31.67 V/\( \mu \)s and power dissipation is 3.2 mW. In the paper simulation result gain margin, phase margin, slew rate and power dissipation is very excellent result.
Finally, the push-pull output stage further enhances the gain. The criteria for determining the circuit bandwidth and gain parameters are discussed. The noise and settling behavior of the proposed circuit are also analyzed in this brief. It is identified that the level shifter contributes considerable noise and adds a PZP to the OTA transfer function, which prolongs the circuit settling time. These level shifters are required for a low-voltage (0.8 V) operation. In the case where supply voltage requirement is relaxed, the level shifters can be eliminated. Thus, the noise and settling behavior of the proposed OTA can be further improved.

Three designs of LV OTA topologies have been described. In addition, effect of OTA non-linearities and the challenges posed by them have been discussed. Simulation results comparing the performance of the above-mentioned OTAs have also been presented. It is seen that enhancement of bandwidth and linearity in LV analog circuits may impose stringent constraints on the power consumption thereby, implying that there always exists a trade-off in obtained performance. This trade-off depends on the specific application at hand. The above-mentioned OTAs can typically be applied to LV analog signal processing applications. OTA-1 has been further used in the implementation of spectral shaping filters conforming to the requirements for HDSL-2. At this time the OTAs operate at 3.3 V supplies. Future work consists of implementing these at lower supply voltages.

This study enriches the existing knowledge on current conveyor based precision rectifiers by presenting two new circuits, each based on two active elements and two MOS transistors, which outperforms the most recent work [5], and the references cited therein. The new circuits benefit by exhibiting high input impedance, resistor-less realization, and simpler & parasitic insensitive topology, making them ideal for integration in CMOS technology. The new circuits exhibit good precision and high frequency operation. Non-ideal study is also given along with attractive computer simulation results. Incorporation of a buffer at the output is an area under investigation for future communication.

This paper have shown how geometric programming can be used to design CMOS op-amps. The method is very efficient, can handle a wide variety of constraints and provides globally optimal designs. Even with relatively simple transistor models, we achieve good agreement with SPICE simulations based on sophisticated models. We are currently developing more sophisticated and accurate models, that are compatible with geometric programming design, and are very accurate even for submicron, short channel designs [2]. GPCAD can also be effectively combined with a (local) optimization method that uses more accurate model equations, or even circuit simulation (such as DELIGHT.SPICE). Thus, GPCAD is used to get close to the (presumably global) optimum, and the
The final design is tuned using the more accurate model or direct circuit simulation. This would reduce the search time of the local optimizer considerably while still preserving extreme accuracy. We mention here several important features that space limitations did not allow us to mention above. When the geometric program is solved, we get a complete sensitivity analysis of the problem, without any additional computational effort. These sensitivity numbers provide extremely useful information to the designer; it shows which constraints are ‘most’ binding; which constraints can be relaxed to obtain a great improvement in the objective function, and which constraints can be tightened without much cost.

IV. COMPARISON OF VARIOUS OTA PARAMETERS:

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.18µm</th>
<th>0.35µm</th>
<th>0.18µm</th>
<th>0.35µm</th>
<th>0.5µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.8V</td>
<td>3.3V</td>
<td>0.8V</td>
<td>1.25V</td>
<td>5V</td>
</tr>
<tr>
<td>Power</td>
<td>1.3mW</td>
<td>3.2mW</td>
<td>0.25mW</td>
<td>0.25mW</td>
<td></td>
</tr>
<tr>
<td>No of PMOS Transistors</td>
<td>4</td>
<td>4</td>
<td>10</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>No of NMOS transistors</td>
<td>3</td>
<td>3</td>
<td>8</td>
<td>10</td>
<td>4</td>
</tr>
<tr>
<td>Total No of Transistors</td>
<td>7</td>
<td>7</td>
<td>18</td>
<td>22</td>
<td>6</td>
</tr>
<tr>
<td>Gain</td>
<td>47.86dB</td>
<td>46.75dB</td>
<td>62dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Margin</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phase Margin</td>
<td>217.53°</td>
<td>225°</td>
<td>670°</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>37.58V/µS</td>
<td>31.67V/µS</td>
<td>160MHZ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CONCLUSION

This paper compares the various designs of OTA. It also compares OTA parameters such as power supply, Gain, Gain Margin, Phase margin, Slew rate for various designs.

REFERENCES


[2] Hitesh Modi, Nilesh Patel, ”Design and simulation of Two stage OTA using 0.18 µm and 0.35 µm Technology”, International Journal of Engineering and Advance technology (IJET) ISSN:2249-8958, volume-2,issue -3,February 2013

[3] Tsung-Hsien Lin, Member, IEEE, Chin-Kung Wu, and Ming-Chung Tsai, “A 0.8-V 0.25-mW Current-Mirror OTA With 160-MHz GBW in 0.18-µm CMOS”, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS


[5] Deyasini Majumdar” Comparative Study Of Low Voltage OTA Designs”
