DESIGN AND IMPLEMENTATION OF AIDED ACQUISITION AND LOCK INDICATION FOR DIGITAL PHASE LOCKED LOOP

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Abstract- Digital PLL allows us to use digital signal processing techniques to improve settling characteristics of the loop. Acquisition is a mode of operation of the PLL during which the PLL acquires lock against the provided input. The most popular way to aid loop acquisition is by sweeping the local NCO or input frequency over a frequency uncertainty window which is centered around an estimate of incoming signal frequency. Lock indication is also an additional feature associated with the subject of acquisition. Once the signal is acquired and input-output are locked, the sweeping circuitry can be disconnected based on a signal from a Lock Indicator circuit. The proposed project implements DPLL which works around the centre frequency 1 kHz, input bandwidth of 1000Hz and sweep bandwidth of 200Hz on either side of the centre frequency with the acquisition time of 40ms. The Digital PLL system is modelled using SIMULINK, simulated on Questa Sim and is then implemented on Virtex-4 FPGA board.

Keywords- Digital PLL, NCO Sweeping, Input Sweeping, Lock indicator, FPGA Virtex 4 module

I. INTRODUCTION

Digital PLL allows us to use digital signal processing techniques to improve settling characteristics of the loop. A simple DPLL will contain three major components; the phase detector, the numerically controlled oscillator (NCO) and loop filter. A major parameter that determines the extent to which the input frequency can be locked is the lock range. The lock range is the range of frequency on either sides of the centre frequency of the NCO through which the input may vary.

If the input falls beyond the lock range, the DPLL may either not lock the input or it may lock the input much later than the acquisition time. In either cases the working fails to satisfy the design.

Frequency sweeping is used to mitigate this shortcoming. The NCO output frequency is controlled by the input. The frequency sweeping circuit acts as an auxiliary input to the NCO and thus sweeps the NCO such that the frequency difference between the input and centre frequency falls within the lock range of the PLL. Sweeping can manifest in two forms. When it is possible to control the input, it can be swept to the lock range, and hence named Input sweeping.

This is applicable in a satellite scenario, where the satellite is expected to receive the input signal. The input signal is in turn controlled by the ground station. When the NCO is controllable, as in the case of a ground station which receives input from a satellite. Then, it is advisable to sweep the NCO.

The Digital PLL (shown in figure 1) is a essential component of almost every coherent receiver system.

The blocks that succeed the PLL in the receiver system wait for the PLL to achieve lock. The lock indicator circuit informs these blocks about the lock.

The paper is organized as follows, section II gives an insight to frequency sweeping and its role in aiding acquisition. Section III explains the lock indicator circuit, which is an additional feature. The real time test results are included and in section IV and section V concludes the paper.

II. FREQUENCY SWEEPING

DPLLs designed to meet precise acquisition time requirements, can be enabled to acquire frequencies beyond the lock range using frequency sweeping[1].

There are two types of frequency sweeping : open loop and closed loop frequency sweeping[2]. In either types, a positive ramp is used if input frequency is lesser than NCO frequency. Else a negative ramp is used[7]. In case a digital scenario, ramp is replaced by a counter. The PLL can sweep and lock efficiently provided the condition for sweep rate is met. That is,

\[ \text{Sweep Rate } R << \frac{\omega_n^2}{2} \quad \text{(1)} \]
The open loop frequency sweeping technique enables a higher sweep rate to be used and requires the sweep generator that has rapid response so that the sweep is disabled before the NCO frequency overshoot occurs.

The closed loop frequency sweeping technique, contains a closed loop during search operation and hence eliminates the need for switching circuitry. The configuration works in a way such that the frequency ramp draws the frequencies together.

A. NCO Sweeping

NCO sweeping is employed when inputs to the system are unpredictable and the NCO has to be swept in order to capture the input[8]. NCO sweeping can be implemented using open loop frequency sweeping, as shown in figure 2. This circuit has two loops.

![Figure 2.Block diagram of NCO sweeping](image)

The inner loop is a simple Phase Locked Loop with a limited lock range and works once the outer loop stops. The outer loop is the sweeping circuit which uses a 90° phase shift of the output, a decision filter, a level comparator and a sweep generator, which is controlled by the threshold. The DPLL with NCO sweeping was modelled for the following specifications:

<table>
<thead>
<tr>
<th>Serial no.</th>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Sampling Frequency</td>
<td>8KHz</td>
</tr>
<tr>
<td>2.</td>
<td>Signal amplitude</td>
<td>127V</td>
</tr>
<tr>
<td>3.</td>
<td>$K_P$</td>
<td>8000</td>
</tr>
<tr>
<td>4.</td>
<td>$K_{NCO}$</td>
<td>0.122 Hz/V</td>
</tr>
<tr>
<td>5.</td>
<td>$K_I$</td>
<td>0.0236</td>
</tr>
<tr>
<td>6.</td>
<td>$K_2$</td>
<td>0.000216</td>
</tr>
<tr>
<td>7.</td>
<td>Acquisition Time</td>
<td>40 ms</td>
</tr>
<tr>
<td>8.</td>
<td>$\phi_0$</td>
<td>103.3848 Hz</td>
</tr>
<tr>
<td>9.</td>
<td>Centre frequency of NCO (fc)</td>
<td>1000 Hz</td>
</tr>
</tbody>
</table>

B. Input Sweeping

Input sweeping is simple and implemented using a single loop[8]. It contains decision filter and sweep generator. It is applicable when the input is under control. The input sweeping circuit is as shown:

![Figure 5.Block Diagram of Input Sweeping](image)

DPLL with input sweeping was modelled for the same specifications as NCO sweeping and the Matlab and VHDL simulations are as shown in the following figures:

![Figure 3.MATLAB results for frequency 1040Hz](image)

![Figure 4.QuestaSim results for frequency 1050Hz](image)

![Figure 6. Matlab results for frequency 970Hz](image)
III. LOCK INDICATOR

Lock indication is a unique feature associated with the subject of acquisition. A Lock indicator circuit, decides when the frequency sweeping circuit has to be enabled once the signal is acquired that is phase lock is achieved, this status is indicated and the frequency sweeping circuit is disabled. It is enabled again when the incoming signal frequency varies with the lock range.

The block diagram above gives the implementation of the lock indicator circuit. It consists of a 90° phase shift of output, multiplier, decision filter and lock indicator implemented using a level threshold. The lock indicator circuit is implemented for both inner loop and outer loop in case of NCO sweeping. All simulation results so far contain the lock indicator output.

IV. REAL-TIME TEST RESULTS

The intended digital system was developed on VHDL using Xilinx and verified using simulation tool, Questa sim. The real time testing was successfully done on FPGA Virtex 4 module. The hardware implementation block diagram is as shown:

The FPGA results for NCO sweeping and lock indication are shown below:

The FPGA was programmed by fusing the bit file on the kit and the results were observed on Digital Storage Oscilloscope.

CONCLUSION

The DPLL with sweeping circuit was modelled and implemented for a centre frequency of 1000 Hz and signal amplitudes of 127 V for an acquisition time of 40ms. The same was tested on FPGA Virtex 4 module, and the results were obtained in close coherence to the design. The future works lies in alleviating noise problems that will arise under practical situations where jitter and Doppler effects come into picture. This prototype model can be scaled up to higher centre frequencies, to suit practical applications.

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