DESIGN AND IMPLEMENTATION OF SRAM

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Abstract- Memory arrays are an essential building block in any digital system. Random access memories are of two types namely static and dynamic. Minimum power requirement with minimum area are the key points in the implementation of VLSI circuits. This paper describes the implementation of SRAM considering these requirements. The schematics are drawn in DSCH software and the layouts are drawn in MICROWIND software.

Keywords- Equalizer circuit, pre-charge circuit, sense amplifier and 6t SRAM Design.

I. INTRODUCTION

The basic block diagram of SRAM is given in figure 1. Basic building blocks of any SRAM chip are row and column decoder, precharge and equalizer circuitry, sense amplifiers and bit cells.

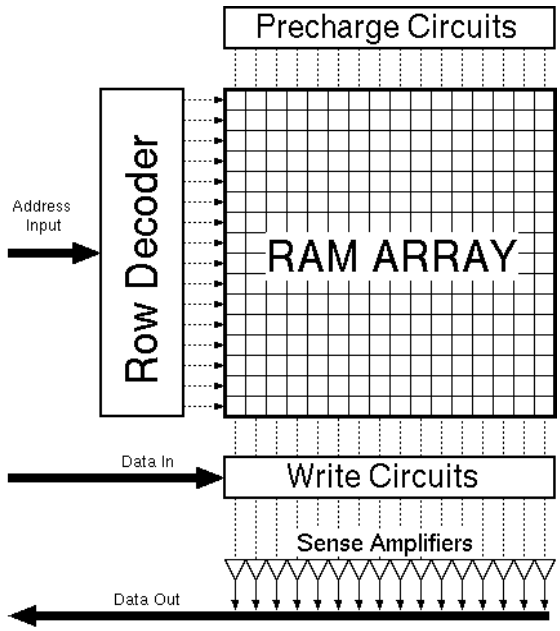

Fig. 1: Block Diagram of SRAM

II. SRAM BIT CELL

The SRAM cell should occupy minimum area to achieve high cell density i.e. number of 1bit SRAM cells per unit area should be as high as possible. Therefore, proper transistor sizing should be achieved. Design parameters should be chosen such a way that Read and Write stability problems are avoided and reliable SRAM chip is obtained. To ensure both read stability and write stability, the NMOS pull-down transistor in the cross coupled inverters must have the highest current carrying capacity, the access transistors are of intermediate strength and the PMOS pull-up transistors must be weak.

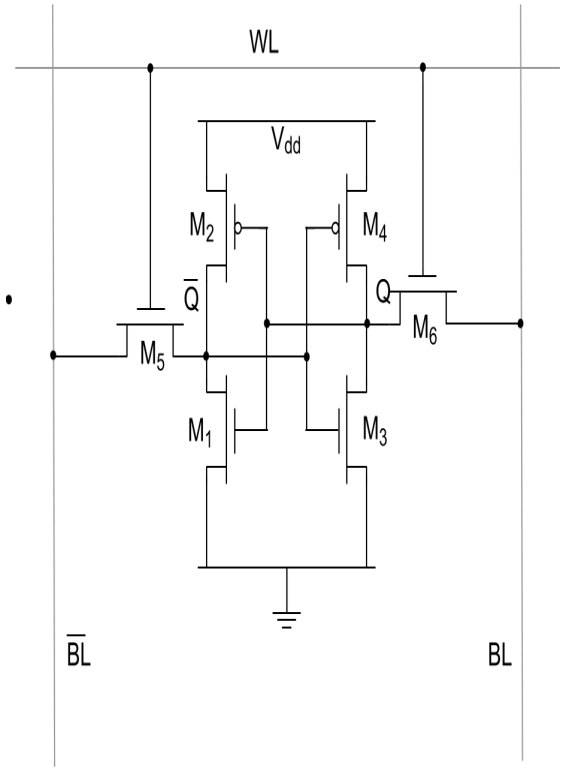

Fig. 2: One Bit Cell

With reference to [2], cell ratio (CR) is the ratio of design parameters of NMOS to the design parameters of access NMOS transistor. CR has to be greater than 1.2 to ensure read stability. A CR value of 1.5 is chosen.

$$CR = \frac{\frac{W3}{L3}}{\frac{W6}{L6}}$$

Similarly, pull-up ratio (PR) is determined to gain write stability. PR value should be less than 1.8. PR value is chosen as 0.8.

Thus widths of PMOS and NMOS transistors are determined.

$$PR = \frac{\frac{W2}{L2}}{\frac{W5}{L6}}$$

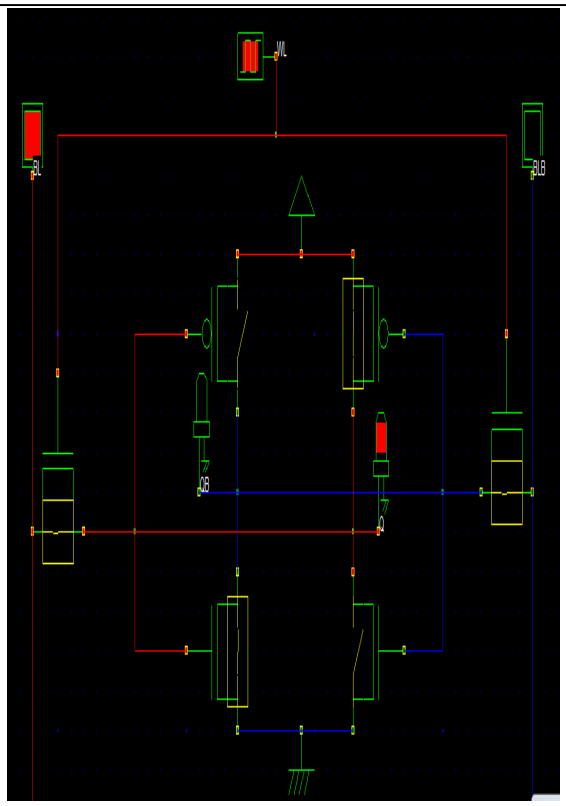

Fig. 3:6T SRAM

When word line is low then bistable latching circuitry is completely isolated from bit lines. Therefore, no change in output is observed during this period. When word line is high then access transistors conduct and bistable latches store a bit. This is observed from output waveforms. When WL is low then Q and Q_BAR both are constant and complement of each other. When WL is high then Q stores the value of BL whereas Q_BAR stores the value of BLB. Therefore, transistors connected to WL are called as Access Transistors.

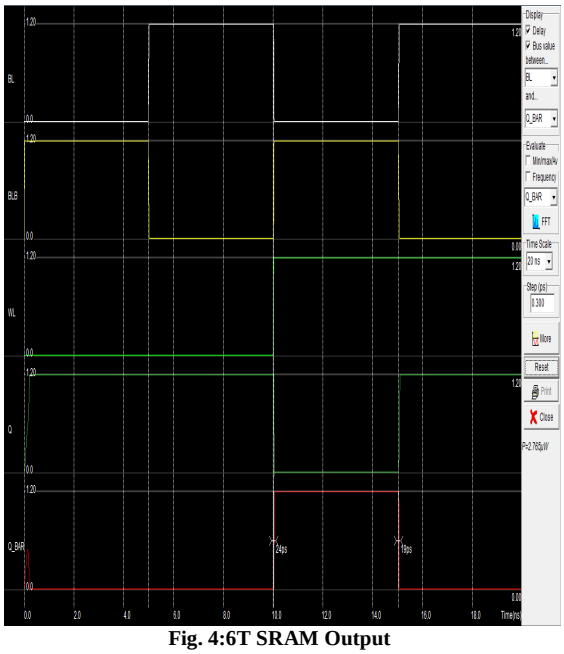

Fig. 4:6T SRAM Output

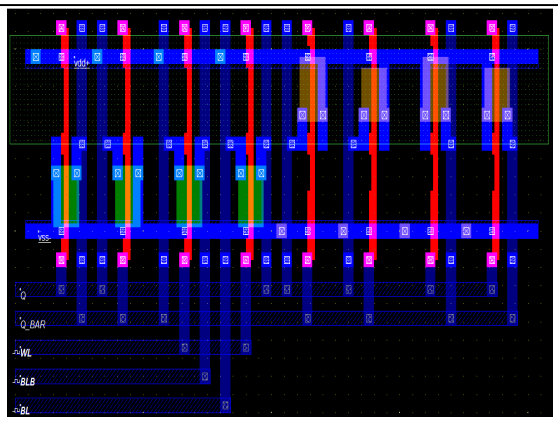

Fig. 5: SRAM layout

III. DECODER

Memory cell matrix consists of rows and columns. Each row is accessed through word line while each column is accessed through bit line. For latching a bit in a memory cell, bit line and complementary bit line both are used. Digit lines or data lines are responsible for transferring the data to and from bit lines depending upon write and read operation respectively. Generally, by making word line high, entire word is obtained. So column decoder is used to distinguish amongst columns. To select a word, row and column addresses must be provided to the decoders. However, row and column decoders are not designed since each bit is accessed individually for testing purpose.

IV. SENSE AMPLIFIERS

Bit stored in a memory cell is determined by the voltage across bit lines. However, due to large number of cells connected to a column circuitry, it is difficult to get proper output. Therefore, sense amplifiers are used as it gives stability and reliability to circuitry. It senses the voltage across bit lines and accordingly, raises or lowers the voltage level. Due to increased voltage level, fan out increases which in turn accelerates bit line transitions. This reduces the delay.

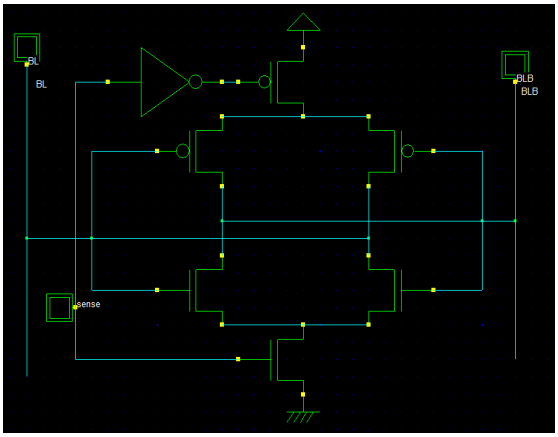

Fig. 6: Cross-coupled CMOS inverter latch used as sense amplifier

In this circuit, sense amplifier is active only when sense input is high. Itconsumes power only when it is activated, but requires a timing sense clock to activate at proper time. When sense clock is high, it turns on the cross coupled inverter pair, which pulls one output low and the other output high through regenerative feedback.

V. PRE-CHARGE AND EQUALIZER CIRCUIT

Before every read and write operation, pre-charge becomes high and both bit lines are charged to a value Vdd/2. During pre-charge and equalizer cycle, both bit lines are shorted so that voltage difference across them is zero.When pre-charge is off and sense amplifier turns on, it senses small voltage difference between two bit lines and accordingly stores a bit in memory cell.

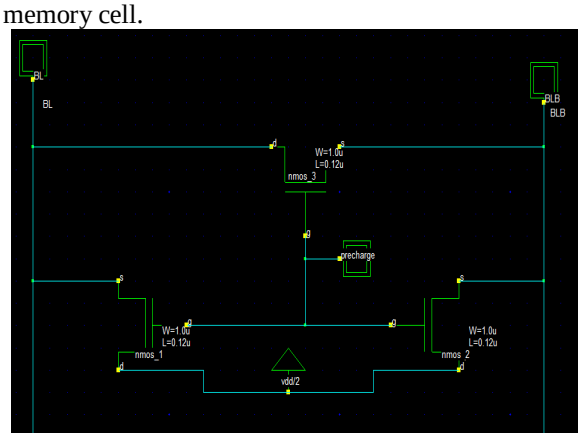

Fig. 7: Pre-charge and equalizer circuit

1-bit SRAM

One bit memory cell is connected with sense amplifier, pre-charge and equalizer circuit. The waveforms of output are shown in fig.10.

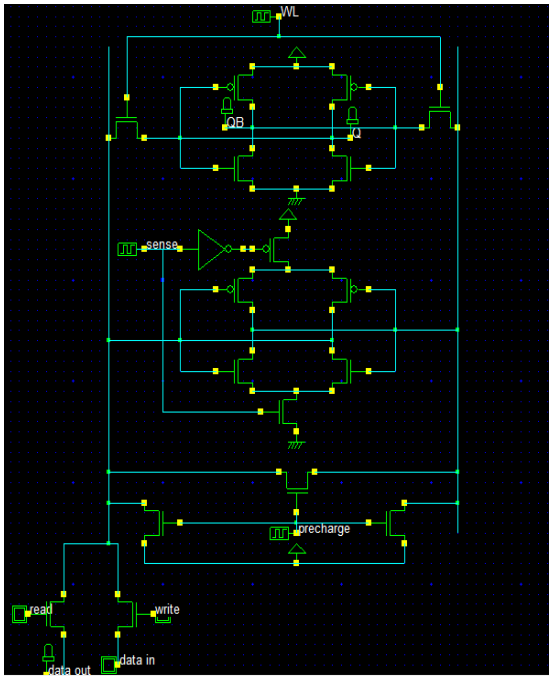

Fig. 8: 1 bit SRAM

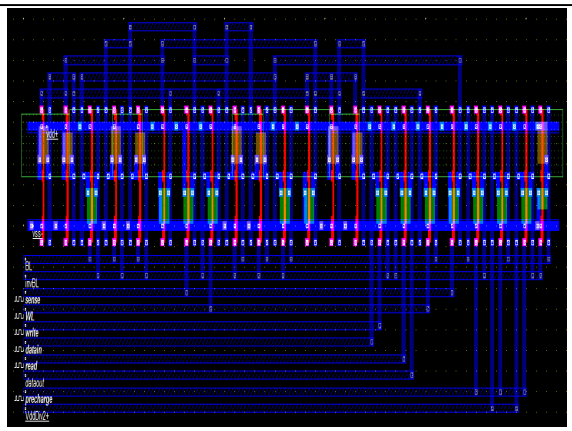

Fig. 9: 1 bit SRAM layout

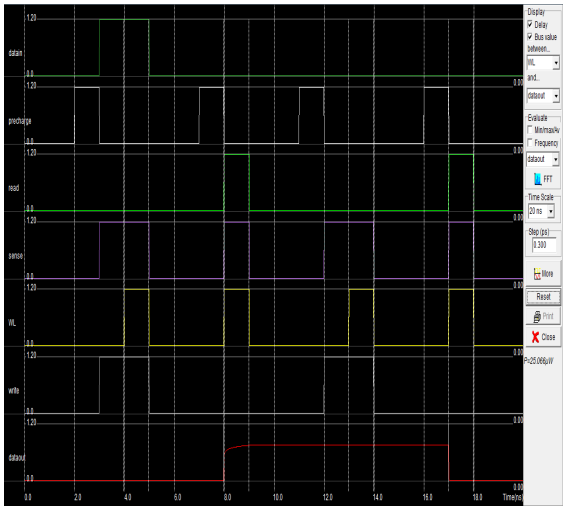

Fig. 10: Output waveforms

Pre-charge and equalizer circuit is activated before write operation. 1 is supplied through datain input signal. Sense amplifier is activated and write enable is provided with high input at the same time. Word line is activated when all inputs are stable. Then to read that stored 1, pre-charge circuit is again activated. Read enable, sense amplifier and word line signal are also activated simultaneously. This turns the dataout signal high.

Similar process is followed for writing 0. Pre-charge and equalizer circuit is activated before write 0 operation. Datain signal is made low and write enable, sense amplifiers and word line are activated. 0 is stored in bit cell. That 0 will be reflected in dataout signal during read operation only. Thus, dataout goes low after read operation.

Complete SRAM

SRAM memory of 8*4 is formed using previous basic concepts. One sense amplifier, one pre-charge circuit and one equalizer circuit is connected to every column.

A pair of bit lines (i.e. BL and BL_BAR) are connected to each column. Word line is common for each row. Thus, entire word could be accumulated during read operation.

There are total 32 bit cells. In our circuit, each bit could be accessed separately for testing purpose.

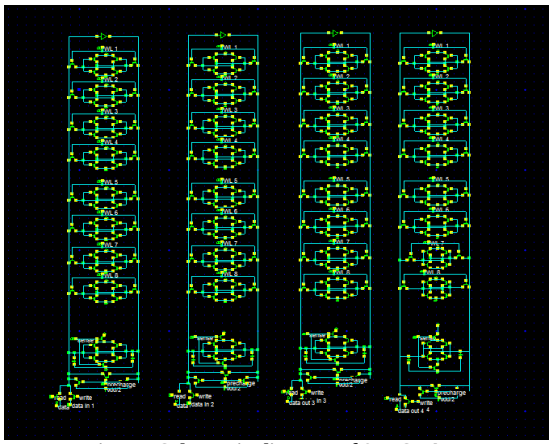

Fig. 11: Schematic diagram of 8*4 SRAM

Output waveforms are quite evident of proper functioning of this SRAM design. Write operation is performed in 20 ns and read operation is performed in 16 ns.

In figure 12, the waveforms of the following operations are shown:-

1. Write '1' at row 2 column 3
2. Write '0' at row 3 column 3
3. Write '0' at row 5 column 2
4. Write '1' at row 7 column 2
5. Read all these values

During write operation, write enabled is high as well as pre-charge circuitry is turned on at proper time. Word Line 2 is active and datain3 is provided high signal. (Note that, data in is connected to bit line.) During read operation, the written 1 is reflected in the dataout3. Then '0' is written at WL3 and datain3 and dataout3 goes low during read operation. Similarly, '0' is written at WL5 datain2 and then output is obtained at dataout2. Finally, '1' is written at WL7 datain2 and dataout2 becomes high during read operation.

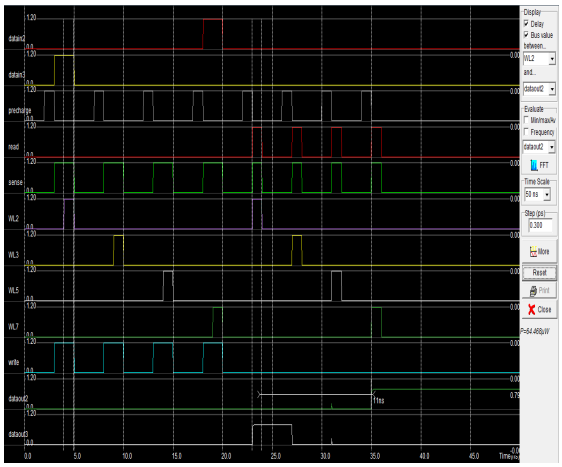

Fig. 12: 8*4 SRAM output waveforms
Power dissipation=64.468uW

CONCLUSION

SRAM memory chip is designed. Widths of transistors should be determined carefully. As width goes on increasing, area of a bit cell increases. Thus number of transistors on the given area decreases i.e. transistor density decreases. However, increasing width of transistors increases current through transistors. Thus power dissipation increases and speed of SRAM increases. Subsequently, delay reduces. Thus, SRAM designing is always a trade of between speed and power dissipation.

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