# DESIGN OF LOW POWER ASYNCHRONOUS 6 TRANSISTOR SRAM IN 45NM CMOS WITH THE USE OF PASS TRANSISTOR BASED TREE DECODERS AND STATIC CMOS BASED TIMING CIRCUITRY ALONG WITH PROCESS VARIATION SIMULATION.

**NIRAV DESAI**

ITM Universe, Vadodara, Gujarat

**Abstract:** This paper describes the design of a 6 Transistor Static Random Access Memory (6T SRAM) in 45nM CMOS along with the design of the peripheral components such as the pass transistor based tree decoders and static CMOS based timing circuit. The basic memory-cell is simulated for read and write- margin variations with a 10% variation in threshold voltage and the complete system design is simulated using test patterns of repetitive 1s and0s. At a clock frequency of 250MHz, the design consumes 28.6fJ/bit.

**Keywords:** 6T SRAM, pass transistor based tree decoder, timing circuit for SRAM, process variation simulations for SRAM, read and write margin for SRAM

## I. INTRODUCTION:

The 6 Transistor SRAM is widely used in Level 1 Cache memories in computers because of its high speed and comparatively lower power dissipation. Pass Transistor based flip flops are preferred for register files which need to be faster than SRAM and the 1 transistor memory cell with charge storage on the gate of the MOSFET is preferred for DRAM because of its lower power consumption. Here the design procedure for a 6 Transistor SRAM cell to be used in the L1 Cache of a microprocessor is introduced along with design of the peripheral circuits for timing and address selection. Low power consumption has been a priority and so pass transistor based tree decoders have been selected due to the lower leakage and dynamic switching currents. An asynchronous design would further help to reduce the dynamic power dissipation from the clock switching [5]. Reliability has been the second important priority and design procedures for high read and write margins tolerant to process variations have been developed. System simulation at transistor level is done using HSPICE on the models provided by NCSU Free PDK. Parasitic estimation is done on the basis of the ASU PTM website data and process variation simulations account for 10% change in threshold voltages. Layout, DRC and LVS were however not carried out due to the lack of sufficient time.

## II. DESIGN:

The basic 6 transistor SRAM cell consisting of 2 cross-coupled inverters is highlighted below.

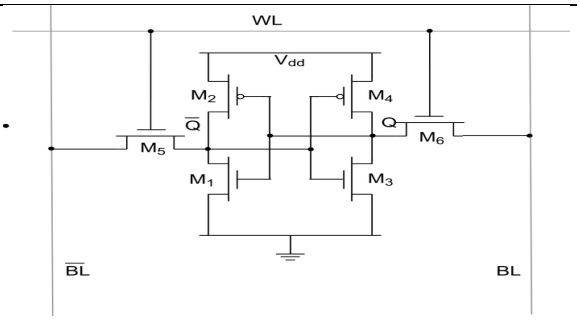


**Figure 1: M1, M3 are inverter pull down transistors. M2 and M4 are inverter pull up transistors. M5 and M6 are NMOS access transistors. BL is bit line and WL is word line. Source: Wikipedia**

The design criteria in the design of the 6T SRAM Cell are [1. Design of High Performance Microprocessor Circuits by AnanthaChandrakasan]**1.) Read Operation Stability:** The NMOS pull down in the inverter should be large enough to discharge the pre-charged bit line through the NMOS access transistorwithout raising the cell node voltage beyond the inverter switching threshold. The Cell Ratio (CR) is defined as the ratio of W/L ratios of NMOS access and NMOS of the inverter.

$$Cell\ Ratio = \frac{Waccess/Laccess}{Wpulldown/Lpulldown}$$

$$> 1.28\ (Read\ Stability\ Equation)\ldots(1)$$

**2.) Write Operation Stability:** The PMOS pull up of the inverter should be small enough so that the bit line driver can flip the cell bit through the NMOS access transistor and write a 0. Mathematically,

$$Pullup\ Ratio = \frac{Wpullup/Lpullup}{Waccess/Laccess}$$

$$< 1.6V\ (Write\ Operation\ Stability)\ldots(2)$$

**3)Minimum Cell Area:** This condition would dictate that the minimum channel length be used for the NMOS access transistor. However, increasing the channel length can give a higher current [2Reverse

Short Channel Effect] and so a channel length little larger than the minimum is preferred. These conditions give a unique design solution for the 6 Transistor SRAM cell for a given technology node. The read circuit uses a sense amplifier (Figure 2) connected in a positive feedback configuration so that a small differential in bit line voltages sensed by the amplifier will get amplified by the positive feedback of the circuit [3].

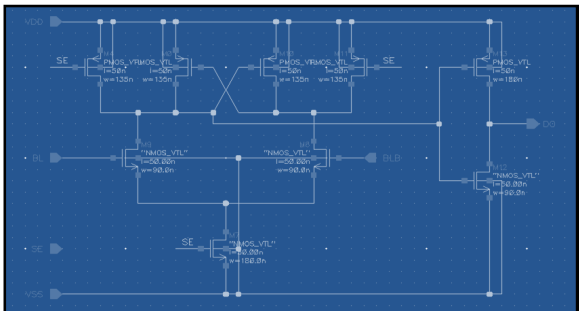

**Figure 2: Sense Amplifier with positive feedback for reading the differential voltages on bit line**

The line drivers (Figure 3) are tri-state buffers that can be disconnected in the read operation.

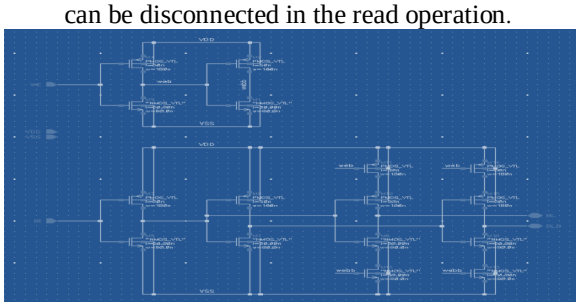

**Figure 3: Line driver with tri-sate output to disconnect it from the bit-line during read operations**

A pass transistor based tree decoder (Figure 4) was designed for this SRAM as it has low static and dynamic leakage.

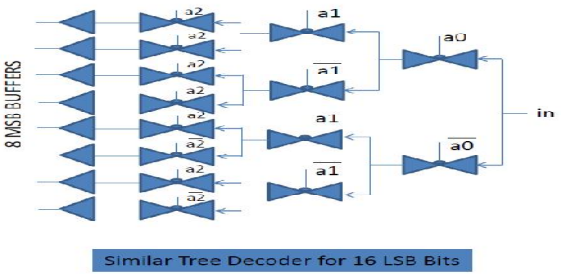


**Figure 4: 1:8 Pass transistor based tree decoder[3]**

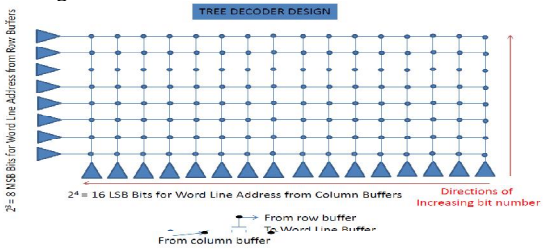


**Figure 5: 7:128 Pass Transistor based tree decoder has low static and dynamic leakage power.**

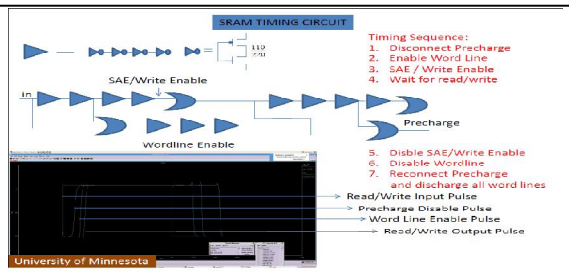


**Figure 6: Self Timed SRAM Timing Circuit designed using static CMOS**

## III. SIMULATION RESULTS:

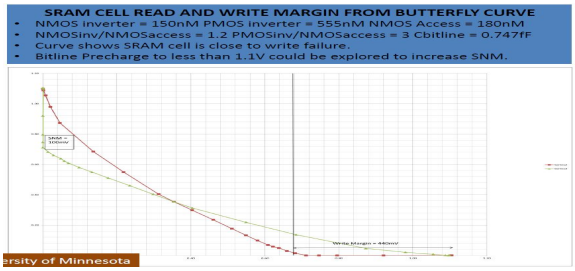


**Figure 7: SRAM Cell Read and Write Margins measured from the butterfly curve. The 2 curves indicate 1 to 0 and 0 to 1 transitions. The Static Noise Margin measured as the size of the largest square that can fit inside the butterfly curve is a 100mV.**

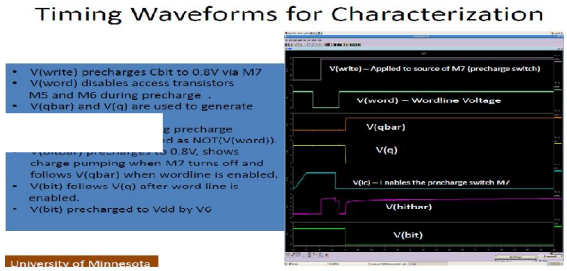


**Figure 8: Timing Waveforms for simulation setup in SRAM characterization for SNM**

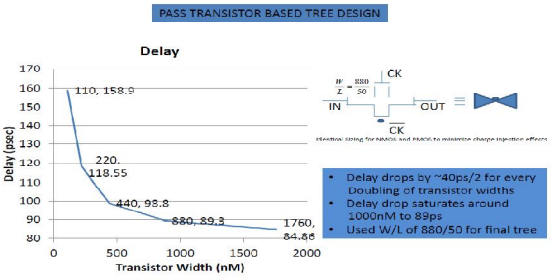


**Figure 9: Pass Transistor Characterization for tree decoder design**

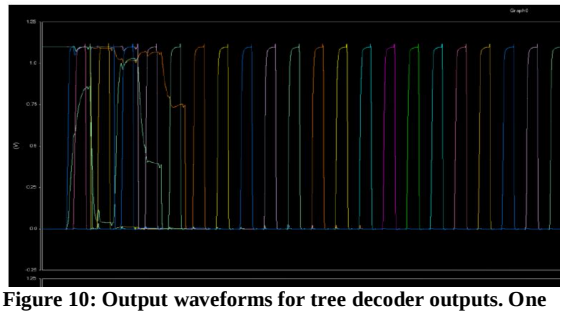

**Figure 10: Output waveforms for tree decoder outputs. One cycle needed to clear all the charged nodes.**

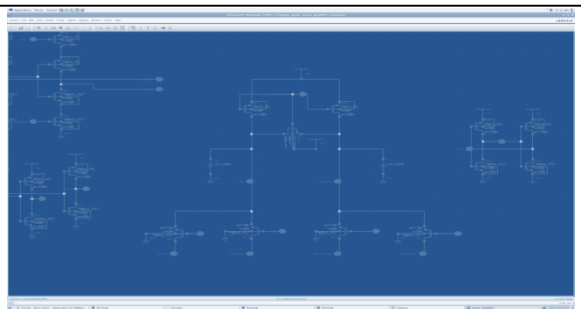

**Figure 11: Read -Write Circuit Test Setup to simulate process variations.**

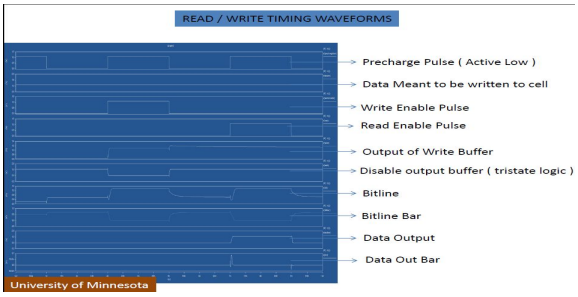


**Figure 12: Read Write Timing Waveforms showing sense amplifier and write driver response.**

## IV. RESULTS:

The SRAM simulations were carried out using a cycle time of 4ns (clock frequency of 250MHz) and calculated power dissipation ($E = V_{supply} \int_0^T I\,dt$) is 28.6 femtoJoule/bit in average case of process variations and 46.2 femto Joule/bit in worst case of process variations (figure 15). This is indicated in the attached figures.

### Implementation and process variation simulations:

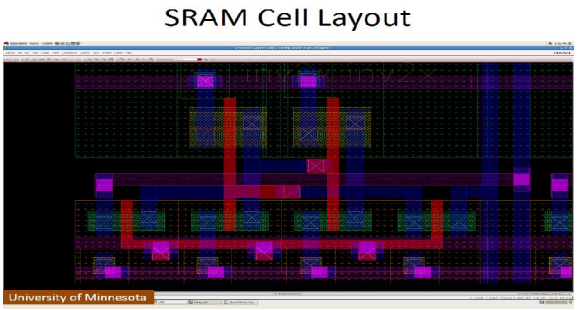


**Figure 13: 6T SRAM Cell Layout in the NCSU Free PDK**

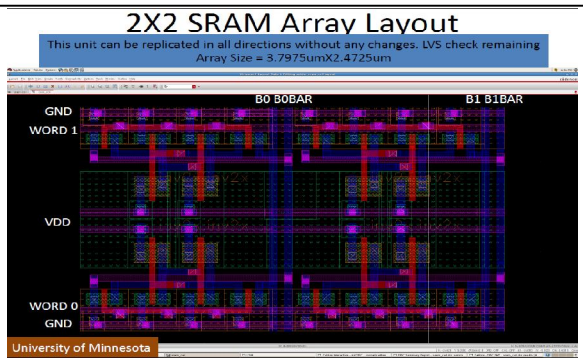


**Figure 14: 4 cell layout for 6T SRAM that can be mirrored in all the directions**

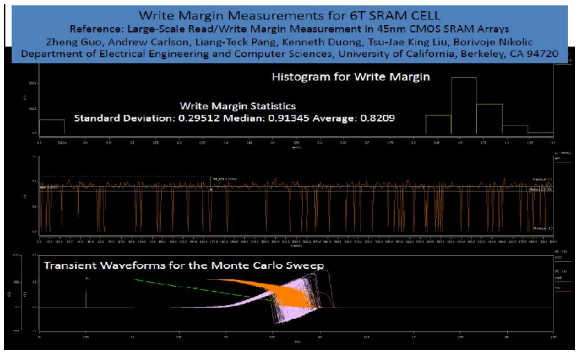


**Figure 15: SRAM Process Variation Monte Carlo simulations indicate that the design works under 10% Vt variation**

## REFERENCES:

[1] Design of High Performance Microprocessor Circuits by Anantha Chandrakasan, William Bowhill, Frank Fox.

[2] A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual-Ground Replica Scheme Tae-Hyoung Kim, Jason Liu, John Keane, Chris H. Kim, University of Minnesota ISSCC 2007.

[3] Digital Integrated Circuits by Jan Rabaey

[4] Large-Scale SRAM Variability Characterization in 45 nm CMOS ZhengGuo, Student Member, IEEE, Andrew Carlson, Member, IEEE, Liang-Teck Pang, Member, IEEE, Kenneth T. Duong, Tsu-Jae King Liu, Fellow, IEEE, and BorivojeNikolic´, Senior Member, IEEE IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 11, NOVEMBER 2009.

**[5]** Dama, J.; Lines, A., "GHz Asynchronous SRAM in 65nm," *Asynchronous Circuits and Systems, 2009. ASYNC '09. 15th IEEE Symposium on* , vol., no., pp.85,94, 17-20 May 2009 doi: 10.1109/ASYNC.2009.23

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