DESIGN OF KOGGE-STONE FOR FAST ADDITION

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Abstract- In this paper, we propose a Kogge-Stone Adder (KSA) with low power consumption and delay. Usually, Ripple Carry Adders (RCA) are preferred for addition of two N-bit numbers as these RCAs provide fast design time among all types of conventional methods. However, RCA's have limitation that every full adder blocks must wait till carry bits generated from previous blocks of full adder. In this paper we implemented Kogge-Stone Adder which is a parallel prefix form Carry Look Ahead (CLA) adder. Parallel prefix adders (PPA) are tree based structure which speed up the binary addition. Hence prefix adders are used for fast addition algorithms. The experimental result shows that the addition by using Kogge-Stone Adder reduces power consumption and delay in comparison with other conventional logics.

Key Words- Parallel Prefix Adder, CLA, RCA, delay, Power Consumption.

I. INTRODUCTION

In processors and in digital circuit designs, adder is an important component. As a result, adder is the main area of research in VLSI system design for improving the performance of a digital system. The performance depends on power consumption and delay. In VLSI technology, parallel prefix adders are known to be efficient. Adders are not only used for arithmetic operations, but also for calculating addresses and indices.

Adders use the combinations of logic gates to combine binary values for obtaining the sum. The adders are sub divided according to their ability to accept and combine the digits. Parallel-Prefix adders perform parallel addition i.e. more important in microprocessors, DSPs, mobile devices and in other high speed applications. The reduction of logic complexity and delay by the Parallel Prefix Adders enhance the performance with factors like delay and power. Therefore the Parallel- Prefix adders are the suitable element in the high speed arithmetic circuits.

II. RIPPLE CARRY ADDER

The Ripple Carry Adder is used for the addition of two N-bit numbers. It consists of N number of full adders for the addition of N-digits numbers. From the next full adder block, carry input of each and every full adder gives the carry output of its previous full adder. This type of adder is typically called as Ripple Carry Adder. It is so called because carry ripples to next full adder. The layout or 3-bit ripple carry adder is shown in Fig 1.

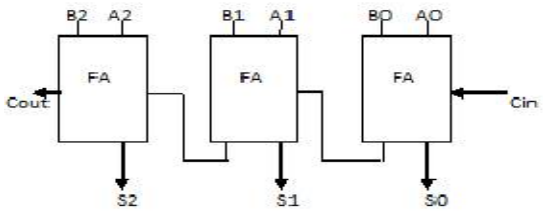

Figure 1: 3-bit Ripple Carry Adder

The major problem for binary addition using RCA is the carry chain. Increasing the input operand width, increases the carry chain length. The worst case occurs when the carry travels the lengthened possible path starting from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). In order to reduce the delay in RCA (or) to propagate the carry in advance, we considering for carry look ahead adder. Basically this type of adder works on two operations called propagate and generate. Increasing the adder bit width, increases the carry complexity. So higher bit CLA designing becomes complexity. In order to compute the carry in prior without delay and complexity, there is a idea called Parallel prefix approach.

III. PARALLEL PREFIX ADDERS:

The delay of Carry-Look Ahead adders can be resolved by employing the scheme of parallel-prefix adders. This concept is to compute small group of intermediate prefixes and then by finding the large group of prefixes, until all the carry bits are computed.Parallel- prefix computation carries out three vital steps is given below:

1) Compute generate & propagate signals by using no. of input bits.
2) Calculate all the carry sequence in parallel that is called prefix computation.
3) Evaluate the final sumof given inputs.

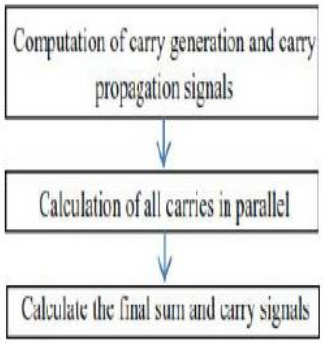

Figure 2: Parallel Prefix Adder Computation

Parallel Prefix Adders basically consists of 3 stages.

1. Pre- processing stage
2. Carry generation network
3. Post processing stage.

1. Pre-Processing Stage:

At this position we compute, generate and propagate signals to the pair of each inputs A and B. These signals are given by the logic equations 1&2.

$p_i = A_i$ x-or B_i …….(1)

$g_i = A_i$ and B_i …….(2)

2. Carry Generation Network:

At this stage we calculate carries corresponding to each bit. The Execution of these operations is carried out in parallel manner. Carry propagate and generate are used as an intermediate signals.The logic equations for carry propagate and generate are shown below.

$P_{i:j} = P_{i:k}$and $P_{k-1:j}$ ……(3)

$G_{i:j} = G_{i:k}$ or ($P_{i:k}$and $G_{k-1:j}$) …..(4)

Black/gray cells implement the given two equations, which will be usually used in the following discussion on prefix trees.

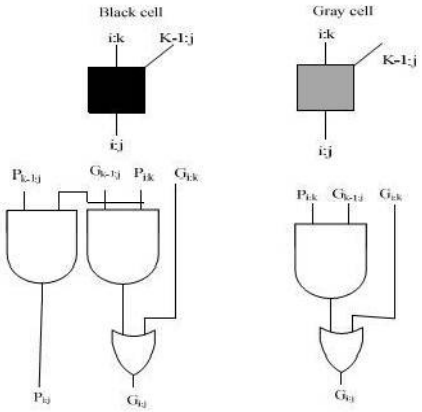

Figure 3: Gray Cell & Black Cell

3. Post Processing Stage:

To compute the sum bits for the given input bits,the logic equationsused are given below.

$C_i = (P_i$ and $C_{in})$ or G_i ……(5)

$S_i = P_i$ xor C_{i-1} ……(6).

IV. KOGGE-STONE ADDER:

Kogge-stone adder is a parallel prefix formation of Carry Look-ahead Adder. Kogge -Stone adder can be showen as a parallel prefix adder consisting of carry operator nodes. It is the fastest adder with based on designing time. It is the common choice for high performance adders in industry. The Kogge-Stone Adder was first developed by Peter M. Kogge and Harold S. Stone in 1973. The construction of 2, 4-bit Kogge-Stone Adder are shown below.

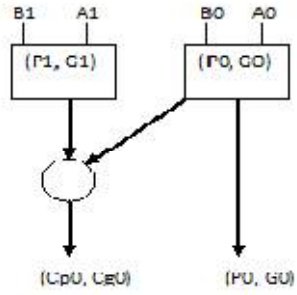

Figure 4: 2-bit KS Adder

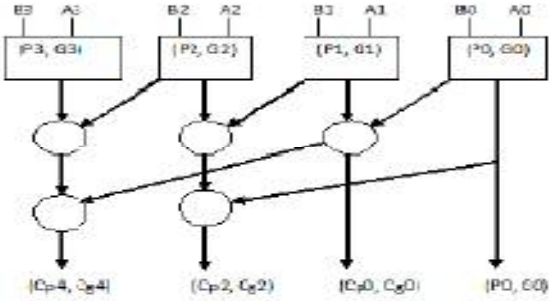

Figure 5: 4-bit KS Adder

The schematic diagram of 16-bit Kogge-Stone Adder was shown in Fig 6.

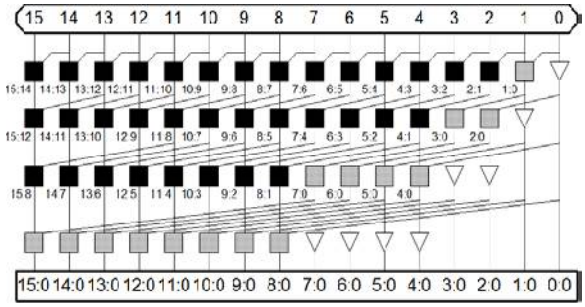

Figure 6: 16-bit KS Adder

The 32-bit Kogge stone construction structure and pin diagram designed using cadence software is shown in Fig 7 & 8.

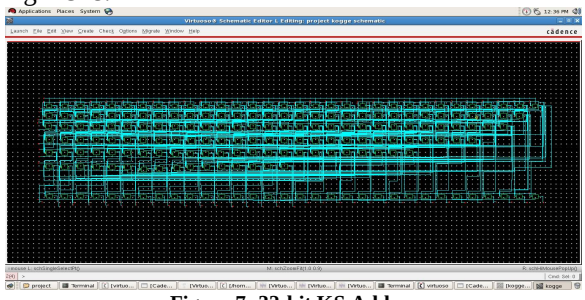

Figure 7: 32-bit KS Adder

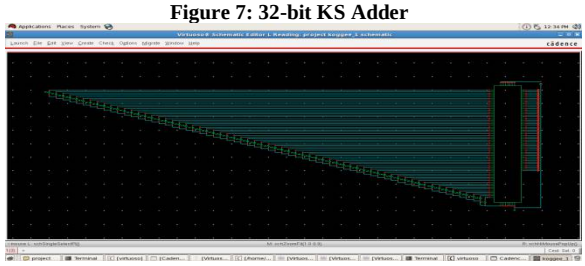

Figure 8: Pin Diagram of 32-bit KS Adder

V. SIMULATION RESULT:

The 32-bit Kogge-Stone Adders was synthesized using Cadence Encounter with TSMC 45nm technology nodes. In this section the synthesis results of 8-bit and 32-bit Kogge Stone Adder are presented in Fig 9 and Fig 10 respectively.

Figure 9: Simulation Result of 8-bit KS Adder

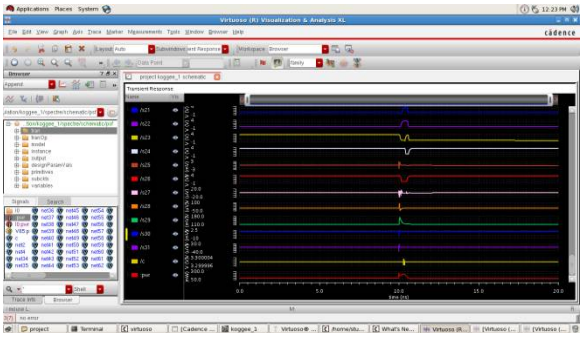

Figure 10: Simulation Result of 32-bit KS Adder

The average power consumption of 8-bit &32-bit Kogge-stone Addersynthesized using Cadence Encounter with TSMC 45nm technology nodes were 6.888E-6, 90.73E-3 respectively.

CONCLUSION

The primary objective of this paper is to design, implement and analyses the performance of 32-bit Kogge-Stone Adder. The performance analysis was based on the power consumption and the worst case delay in performing the operation. In this paper the CMOS adders were realized using TSMC 45 nm technologies. The result shows that the proposed KSA greatly reduces the power consumption.

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